# K. Shiva kumar

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## Profile

Analog layout engineer with 3 Years of experience in custom layout design. I have worked on current technology nodes for High Speed SerDes sub blocks, OP-AMP, Bandgap Reference, and DAC.

**Technology Node Hands On:-#Intel (7nm, 10nm) #TSMC (45nm, 130nm) Technology.**

## Area of Interest

**#ANALOG LAYOUT DESIGN, #MEMORY LAYOUT DESIGN, #ESD (LAYOUT DESIGN).**

## Awards and Recognition

- Execution Excellence for completing a Process Monitor IP with minimal efforts from peers independently **(QORVO_AD1513_SoC)**
- Customer Excellence for completing the task on time with quality from **INTEL** (October 2022).

## Education

**BACHELOR OF ELECTRONIC & TELECOMMUNICATION | JUNE 2018 | MALLA REDDY COLLEGE OF ENGINEERING (MRCE), TELANGANA |Percentage: 73% (Grade: 1st Class)**

## Technical Skills

| | |
|---|---|
| EDA tools | Cadence Virtuoso (L, XL & EXL)/Schematic Editor, Synopsys Compiler. |
| Verification tools | Calibre, Synopsys ICC2, Assura, Argon, Totem. |
| Process Technology | TSMC45NM, TSMC130NM, INTEL7NM & INTEL10NM. |
| OS Platforms | Linux, Windows. |

## Experience (3 Years – Analog Layout design)

**DESIGN ENGINEER | SANKALP SEMICONDUCTOR PVT LTD | JANUARY 2021 - PRESENT**

- **Technology Hand's on Experience**: Intel (7nm & 10nm), TSMC45nm, TSMC130nm.
- Worked on analog sub blocks for High speed SerDes (worked Analog and critical digital sub blocks of SerDes).

## Project1: QORVO_AD1513_SoC (TSMC45nm)

- Layout development of various analog and digital sub-blocks.
- Tools Used: Cadence Virtuoso, Calibre.
- Complete ownership of following block.
- Error Amplifier => Floorplaning, Placement and Routing
- Constraints
  - ✓ DIFF Pair and Current Mirror Symmetrical Routing
  - ✓ Taking care all the Latch-up related error with respect to PAD connected device
  - ✓ Resistor Matching.
  - ✓ Strong robust connection for power.
  - ✓ Shielding of Bias signal

## Project2: Ethernet_UX3.1 (INTEL-10nm)

- Layout development of level shifters and ESD clamps.
- Tools Used: Cadence Virtuoso, Synopsys ICV, Totem, Argon.
- Roles & Responsibilities:
  - ✓ Responsible for layout implementation of level shifters and ESD blocks.
  - ✓ Coordinated with designers in ECO/LCO implementation.
  - ✓ Worked on RV cleanup for assigned blocks using Totem tool & hands-on experience of totem tool for RV violation analysis and fixes.
  - ✓ Worked on Physical verifications like DRC, LVS, density, PROD bundle cleanup.
  - ✓ Hands-on usage of Argon tool for resistance and cap matching for routes.
  - ✓ Implemented test cases and documented critical issues/errors within layout.
  - ✓ Coordinated with QA team for RV, HV, LV bundle flow data status & responsible for on time closure of HSD tickets.

## Project3: DP_GEN3 (INTEL-7nm)

- Layout development of Comparators.
- Tools Used: Cadence Virtuoso, Synopsys ICV, Totem, Argon.
- Roles & Responsibilities:
  - ✓ Responsible for layout implementation of comparator block.
  - ✓ Floor planning, Placement, Routing, Post layout Fixes.
  - ✓ Completion of blocks with minimal escalations in deadlines and maintaining quality.
- Challenges:
  - Understanding the 7nm DRCs, delivering blocks with quality on time.
  - Maintaining VXL compliance, Matching Check, Missing Via checks. Parasitics capacitance constraint on all nets in high speed Digital Blocks.
  - Symmetrical Routing using cloning and synchronous copy to meet layout constraints.
  - Fixing EM and IR for critical signal in blocks.

## Project4: Analog & Digital Sub blocks of PMIC (HCL internal)

- Layout development of various analog and digital sub blocks for Power Management Unit
- Process and Technology Used: TSMC130nm, Cadence Virtuoso, Calibre.
- Responsibilities: Floor planning, Placement, Routing, Verification and Post layout fixes (if any).
- Challenges:
  - Understanding the 130nm DRCs, delivering blocks with quality on time.
  - Routing of all the blocks to be completed in maximum 3 metals.
  - Symmetrical routing by meeting constraints.
  - Minimum 2 Via constraints for every connection.

## Declaration

I hereby declare that the above-mentioned details are true to the best of my knowledge and consideration.

**Dated:**

**K. Shiva Kumar**