SHASHANK LINGALA
Curriculum Vitae
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PERSONAL DETAILS

Name : SHASHANK LINGALA
Date of birth : 22nd January,1987
Place of residence : Hyderabad, INDIA

PROFILE & AMBITION

I am an Analog IC design engineer from INDIA. My introduction to IC design was during graduation where I was associated with RFIC and Microwave devices laboratory. I had an opportunity to work through the complete IC design cycle from design, layout and testing of the prototype design of CMOS ring oscillator. Since then, I have been working in Analog CMOS IC design on various technology nodes.

My ambition for the near future is to grow expertise in the Analog signal chain domain and also to develop experience in the product development cycle of an IC.

WORK EXPERIENCE

	Period	**Department and function**
Luminasic Pvt. Ltd., India	2018 ~present	Analog IC design engineer
Digicomm Semiconductors Pvt. Ltd., India	2017 ~ 2018	Analog IC design consultant
Elveego Circuits Pvt. Ltd., India	2013 ~ 2017	Member of Technical staff, Analog
SM Wireless Solutions	2012 ~ 2012	Design engineer

The position is described in more detail in the portfolio

EXPERTISE

	Average	Good	Very Good	Excellent
Operating Systems				
Windows		✓		
Linux		✓		
Cadence Virtuoso				
Schematic L, XL			✓	
ADE L, XL			✓	
Spectre			✓	
Spectre RF		✓		
Layout L		✓		
Mentor Graphics				
Calibre (DRC, LVS)		✓		

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PORTFOLIO

LUMINASIC Pvt. Ltd., Analog Design Engineer
Period: September, 2018 ~ present

- Project: **L**arge **A**rea **V**isible **A**rray ROIC

LAVA is a read out IC for CMOS pixel array of 22500 (H) x 15000 (V). I was assigned two major blocks in the project and apart from them took various other responsibilities as bandwidth permitted.

Tasks:

- Design of Ramp generator (current integration-based architecture).
  - Design programmability to ensure constant slope of ramp across PVT and to meet the linearity specifications as well.
  - Design for reliability considering the large peak current during reset of the integration capacitor.
- Design of 1.5T pixel control signal drivers (Read, Reset, Tx).
  - Design of drivers for very low leakage currents was the real challenge.
  - Design considering use of various level shifters to make sure the voltage across the transistors do not exceed the breakdown voltages.
- Test bench creation for verification of above designs.
- Array level schematic creation and functional verification at array level.
- I guided junior design engineer working on Bias generation blocks.
- I assisted layout engineers with LVS issues and help in developing their understanding of array level labels used in schematic.

Keywords: Level-shifters, low-power, V2I converter, LVS

- Project: **Pipelined Analog to Digital Converter (ADC)**

Pipelined ADC is designed and implemented as 8-channel ADC for readout in low-noise instruments. I had the opportunity to work on switched capacitor circuits in this project and develop an understanding on derivation of block specifciations from system level specs provided. I also worked on porting of pre-amplifier and MDAC stage-1 designs design to other foundry PDK in the subsequent IP development project.

Tasks:

- Bias Generator schematic porting and verification.
- Specification derivation and design of opamp used in Residue amplifier.
- Power scaling of residue amplifier for use in subsequent stages of ADC.
- Comparator verification (& test bench creation) used in Flash ADC.
- Implementation and verification of Digital error correction logic.
- Pad ring design and verification.

Keywords: switched-capacitor circuits, op-amp, pads

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- Project: **TDI Image Sensor ROIC**

Time Delay Integration (TDI) technique is used in low light imaging such as space applications. I had the ownership of Bias generation block and extensive verification of clock, data paths and supply IR drop analysis.

Tasks:

- Design of Ramp generator (current integration-based architecture).
  - Design programmability to ensure constant slope of ramp across PVT and to meet linearity specifications as well.
  - Design for reliability considering the large peak current during reset of the integrat capacitor.
  - I could successfully debug the issue related to leakage during reset and added programmability to mitigate the same.
  - Design modified to increase the voltage swing of the cascode current source.
- Design of Bandgap reference circuit and PTAT current reference generation.
  - Design activity taken up to decrease temperature co-efficient of the BGR.
- Reference buffer design used for references in column-ADC.
- Test bench creation for verification of above designs.

Keywords: BGR, PTAT Bias current, Reference buffer, IR drop, clock buffering

Digicomm Semiconductors Pvt. Ltd., Analog Design Engineer
Period: August, 2017 ~ August, 2018

- Project: **Low Dropout Regulator (LDO)**

I designed a LDO prototype as given in the reference (*ref: IEEE JSSC, Vol. 42, No. 8, August 2007*) and guided Junior design engineers with verification and report preparation by providing them with test benches and verification outlines.

Tasks:

- Implementation of a low quiescent current LDO regulator with Buffer Impedance Attenuation technique.
- Guide junior engineers with implementation and verification (in Tanner EDA tool) and report preparation.
- I also took up the design of Vt/R based power on reset ciruit (POR) and in this project was introduced to project management tools like JAMA, Jira.

Keywords: LDO, POR, JAMA, JIRA

Elveego Circuits Pvt. Ltd., MTS Analog Design
Period: April, 2013 ~ July, 2017

- Project: **CMOS Image Sensor ROIC**

I was placed at SONY, Japan as consultant where I got introduced to the CMOS image sensor domain. Since I had no prior experience in these designs, my responsibilities were mostly limited to verification.

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Tasks:
- Verification of Vertical scanner block
- HISMCCK check for leak paths, TREC and EM analysis.

- Project: **LVDS Transmitter and Receiver design (TIA/EIA-644 Standard)**

Tasks:
- Design and verification of LVDS Transmitter and Receiver buffers in Tower Jazz 180nm CMOS technology node for data rates of up to 945Mbps.
- Design of Built in Self Test (BIST) circuits like fixed pattern generator, PRBS7.
- Verification of Bandgap Reference and LDO regulator over corners.

Keywords: HSIMCCK, EM, POR, LVDS Tx/Rx, verification

SM Wireless Solutions Pvt. Ltd., MTS Analog Design
Period: January, 2012 ~ August, 2012

- Project: **900MHz, Direct Conversion Transceiver Front-end**

Tasks:
- Design of a two-stage folded-cascode operational amplifier with rail-to-rail input common mode range in CSMC 0.13um CMOS technology.
- Design of a programmable gain amplifier (PGA) with low frequency feedback for DC offset cancellation in CSMC 0.13um CMOS technology.

Keywords: Folded-cascode opamp, PGA

PUBLICATIONS

[1] **S. Lingala** et al., "A wide tuning range – 163 FOM CMOS quadrature ring oscillator for Inductor less reconfigurable PLL", IEEE International symposium on Signals, Systems & Electronics 2010, September 17-20, China. ***(Nominated for best student paper award)***

[2] **S. Lingala** et al., "A 1.35-6.15GHz linear voltage-controlled ring oscillator in 180nm CMOS", IEICE Electronics society conference, C-12-33, September 2010, Japan.

EDUCATION

	Education & Projects
Kyushu University, JAPAN	Master of Engineering Graduate school of ISEE **Graduation project**: Design and Implementation of a Low phase noise Ring Oscillator in CMOS 180nm technology
Osmania University, INDIA	Bachelor of Engineering Specialization in Instrumentation Engineering