J A G A N A T H R A J E N D R A

PERSONAL DETAILS

Date of birth:	23 April 1975
Address:	#178, Ramgopal Layout, Banaswadi Main Road, Bangalore-33
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Nationality:	British Citizen

SUMMARY

- 19+ years' experience in CMOS transistor-level design and Layout.
- Expertise in the implementation of analogue and mixed signal full-custom macros from specification to layout.
- Responsible for full chip activity from system specification, system modelling, circuit architecture definition, block level circuit design, close monitoring of layout, extraction simulation and design for testability
- Served as chip lead for a mobile image sensor product. Experience in driving the project from marketing requirement to full product.
- Was involved in complete product development life cycle from specification to qualifying the product to the market.
- Work closely with technology group for ESD reviews for I/O ring for the chip.
- Have strong technical background with hands on transistor level design experience.
- Have background experience in both Research and Product Development.

EXPERIENCE

Jan 2019 – Till Date: **Depixus, Cambridge/Paris** Principal Analogue Design Engineer

- Working towards 1-Billion Pixel DNA sensor chip.
- Highly scalable (Targeting 1-billion pixels) current mode pixel circuits for electro spectroscopy impedance sensor
- Feasibility on scalability in terms of area and power
- Complete column readout noise analysis
- Designed a 13-bit SAR ADC @ 12.5MHz using segmented capacitive DAC
- Implemented CDS for low noise switched capacitor circuit
- Pixel readout system architecture
- Readout chain instrumentation architecture containing column bias, Preamplifier , CDS and ADC

Low noise high

Oct 2015 – Dec 2018: **DNAe Ltd, London , UK**. Principal Analogue Design Engineer

- Worked on a 6-Meg ISFET medical DNA sensor.
- Responsible for designing a highly linear 13-bit SAR ADC using segmented capacitive DAC
- Low noise high gain preamplifier-based comparator design
- ADC feasibility based on capacitor mismatch parameters. Derivation of key specs like power, area and speed using modelling
- Wide input range 400Mhz clock output charge pump PLL design. PLL used to supply clock for LVDS, ADC and LOGIC of the chip
- Research on current mode readout architectures based on continuous time sigma delta ADC.

Sept 2011 – September 2015: **Aptina Imaging/ON Semiconductor Bangalore**

Staff design engineer/Design Engineering Manager, Sensor Design Group

- Worked on a 5MP image sensor. Serving as chip lead and project manager for this project.
- Design of analogue signal chain circuitry: A-to-D converters, bias modules, programmable-gain amplifiers, Level shifter circuits
  - 12-bit 150MHz capacitive DAC ramp generator for column parallel ramp ADC
  - Readout Noise analysis of sensor from Pixel source follower to ADC
- Responsible for wafer level silicon bring up activities
  - Silicon validation on wafer and package parts
  - Root causing image arti-facts to circuits
  - Was chip lead for getting the product from first revision to production worthy
- Worked on 2MP sensor for mobile application. Worked in all phases of the project.
  - Was responsible Ramp DAC design in tsmc 65nm technology for single slope RAMP ADC
  - Was responsible for full chip level schematic creation and functional verification
  - Involved in silicon bring up by probing wafer for all basic analog blocks
  - Involve din post silicon validation and fixed bugs found in metal revision.
  - Worked in validation process to get the product qualified for market

Jan 2011 – July 2011: Design service to **DNAe, London**

Tech Lead:

- Worked on 12-bit SAR ADC for an DNA array sensor (7000 X 7000)
  - Architecture analysis for less area and power
  - Column multiplexing to reduce no. of ADC's
  - Slew rate enhanced folded cascade reference voltage buffer
- Low jitter charge pump PLL to generate ADC clock.
- Temperature Sensor design.

October 2010 – December 2010: MOSCAS Ltd, Oxford

Research Consultant

- Design consultancy to **NXP, Hamburg**
  - Leakage power reduction for smart card product from 200uA to less than 30uA.

May 2010 – October: Design Service to **Sharp Labs, Oxford**

Project Lead:

- CMOS Image sensor readout circuit design.
- Highly linear front end current mode integrator
- Current mode CDS to reduce FPN noise
- Adaptive gain control to improve SNR
- 10-bit low power SAR ADC with capacitive DAC

Sep 2007-2010: **Intel Corporation UK Ltd,** Swindon.

Senior Mixed Signal IC Design Engineer, Tuner and Demodulator Group

- Data converters for DVB-S/H/T in 65nm and 32nm technology.

- Currently working on pierce crystal oscillator design for low jitter & programmable gain control for crystal frequencies up to 41Mhz
- Modelling and feasibility study of IF to baseband (Near zero) conversion for front end of sigma delta ADC using sub sampling and mixer topologies.
- Modules for 12-bit 64MSPS 2.5bit per stage Pipeline ADC:
  - Designing high-speed fully differential capacitance interpolative comparator for sub ADC in MDAC
  - Low jitter fully differential clock tree buffer.
  - Bootstrap sampling switch.
- Design & Development of a 12-bit 200MSPS segmented (9-3) current steering DAC.
  - Verilog-A model was developed to simulate and characterise complete DAC.
- Design and development of low jitter < 4ps PLL to supply clock for ADC:
  - Very low phase noise VCO.
  - Verilog-A modelling to simulate complete PLL for transient and AC response.

Jan 2004 – Aug 2007: **Sharp Laboratories of Europe Ltd**, Oxford.
Senior Researcher/Research Scientist, System Display Group

- Analogue IP design for silicon-on-glass TFT panel technology.
- Projects:
  - PLL-based clock multiplier: 500KHz to 4MHz, fully monolithic, integrated within an LCD panel.
    - Simulink model of charge pump PLL for easy characterisation of loop filter parameters.
  - On-panel DC-DC converter with switched capacitor regulator:
    - Capable of generating a 9V/-4V internal panel supply from an external 5V battery, max power 500uW and efficiency > 70% under a wide range of process conditions.
  - Low power video line buffer design for an LCD panel.
    - Based on a floating current source configuration around a class-AB opamp.
    - Settling time<20us, within 100mV of video DAC output voltage driving 20pF load.
    - Buffer designed in sub-threshold region for low power consumption of <15uW
  - QVGA Analogue panel
    - Design of full monolithic video source and gate drivers for QVGA LCD panel.
    - Two patents filed on new design.
  - On panel Audio module:
    - Two-bit digital volume control to vary the amplitude of audio signal at the input of output buffer.
    - Poster published in EuroDisplay 2005 conference.
  - Comparison of various technology process for analog design trade off
    - Benchmark analysis for optimal operating points suitable for analog design
    - Benchmark analysis to characterise maximum achievable parameters for opamp design like I/O voltage range & open-loop gain

Oct 2002 - Dec 2003: **Renesas Technology Europe Ltd**, Bourne End, Buckinghamshire
Design Engineer, Mixed-Signal Design Group

- Project: 0.18um CMOS analogue cell library for the AE-5 series of smart card microcontrollers (emphasis on low power and low cost)
  - Analysis, Top-level test bench creation & simulations of Smart card Analogue

detector modules for AE-5 series of smart card microcontrollers.

- Low Voltage Low power BICMOS Bandgap Reference of 0.6v with supply-independent biasing
- Complete Top-level layout including floor planning & analogue module integration for AE5-series smart card microcontroller. Routing of Supply, shielding of signals, ESD-protection & Area optimisation were main challenge

Jan 2001 - Oct 2002: **Hitachi Micro Systems Europe Ltd**, Maidenhead, Berkshire

Design Engineer, Mixed-Signal Design Group

- Project: baseband analogue front-end device for GSM (0.35um CMOS process).
- Relevant modules:
  - Differential interface for a BandGap Voltage reference of 1.2v used as reference voltage for Base band chip
  - A voltage multiplier was designed to convert mic bias voltage from 1.2 v to 2V.It contains a signal stage opamp with a voltage divider circuit.
  - Feasibility study, simulink modelling and involved in design activities of Sigma-Delta A/D converters
  - Continuous time 12-bit Sigma delta ADC design
  - Design & Implementation of Folded Cascode Opamp with high DC gain of 90db & very high Unity Gain Bandwidth of 100Mhz with Miller Compensation

June 2000 – Dec 2000 **U&I Scotty computers ltd** Bangalore, India

Trainee engineer, Memory Design Group

- Design & Development of a single transistor DRAM cell & sense amplifier for a MLDRAM (2-bit per cell) with new Sequential Sensing Scheme. The advantage of proposed scheme is to sense four Logical levels using two sense amplifiers.

EDUCATION

1998 - 2000: Bangalore University, India

- MEng Electronics & communication Engineering

1993 - 1997: Bangalore University, India

- BEng Electronics & communication Engineering
- Obtained professional certification
- CEng April-2010: The Institute of Engineering and Technology, London

CAD TOOLS

- Analogue design flow mainly based on Cadence tools: Virtuoso Schematic and Layout (design entry), Analogue Design Environment, ADEXL, ADE-EXPLORER (simulation interface), and Assura and Calibre (layout verification).
- Experience of Cadence SKILL language.
- Experience in high-level analogue modelling with Matlab & Simulink.
- Experience in Mixed signal simulations using Cadence AMS and Synopsys VCS-AMS and XA tools
- Very good knowledge in VerilogA modelling.
- Electrical simulation: Hspice, Spectre and Silvaco SmartSpice.
- Physical verification: Mentor Calibre, Cadence Assura.
- Basic knowledge of digital synthesis and simulation tools: Verilog HDL language.
- Platforms: Unix (Solaris and Linux), Windows

PATENTS & PUBLICATIONS

"Digital logic circuit, shift register and active matrix device" EP09738686

"Drive circuit, a display device provided with the same" US8354990

"Digital logic circuit, shift register and active matrix device" US 8107587

"A 2.4-inch CG-silicon system LCD with a Monolithic Audio Driver" , EuroDisplay 2005