Jagadishkumar L.S.

OBJECTIVE: Seeking a full-time position in the field of Layout Design which would be mutually beneficial in terms of learning, experience and contribution to organization growth

Name	Jagadishkumar L.S.
Designation/Role	Engineer –AMS layout
Total Experience	5.4 years
Email Id	jagadishkumarls@rediffmail.com
Mobile No	+918660709441
Highest Education	M.Tech.
Key Skill Set	**Software** : Xilinx ISE ,ModelSim, MATLAB,Linux, Windows **EDA tools** : Cadence Virtuoso Layout Editor, TSMC Modgen, Mentor Graphics Pyxis, Tanner EDA, Calibre IC verification tool, **Totem tool for RV** **Technology nodes worked**: **TSMC 28nm, 16nm, 5nm, 7nm ,6nm,3nm,22nm**

Academic Profile:

Degree	School/ College/Institute	Board/University	Year of passing
M.Tech.	S.D.I.T. Mangalore	V.T.U.	2015
B.E.	S.T.J.I.T Ranebennur	V.T.U.	2013

Experience Summary:

Role/Designation	Employer	Duration	Years, months
Engineer	Altran India	June 2017 to Oct 2020	3 years 4 months
Senior Engineer-1	HCL	November 2020 –December 2021	1 year 1 month
Engineer –AMS layout	Cyient Ltd.	December 2021-June 2022	6 months
Lead Engineer	Wipro	July 4th -Present	

Profile Summary:

- Good experience in Analog Layout Design. Exposure to verification methodologies like DRC, HVDRC, LVS, ERC, antenna check, parasitic extraction, RV improvements, Cleaning EM.
- Good experience in floor planning, matching of analog blocks.
- Strong knowledge in Layout Design concepts.

Project details:

Project:	**Smarti9**
Location	ALTRAN Technologies, Bangalore
Client	Intel
Contribution:	*Roles and Responsibilities* ➢ Worked many digital blocks and analog blocks in TSMC 16nm technology node(FinFETs) like Mux, Watchdog layout, Op-amp, Level shifters for Intel Israel team and also FBR Bias block, LOPA cells, Top level routing. Done area estimation, floor-planning, matching, Routing and verification checks like LVS, DRC, HVDRC, ERC, soft check. Taken care of many constraints like EM/IR, RC parasitic, and DFM checks. Maintained routing symmetry wherever needed. ➢ Worked on RF blocks in 16nmtechnology. ➢ Worked in TSMC 28 nm Intel project for blocks like Mixer bias, clock tree, clock driver, resistor arrays with layout floor plan, matching, routing and done verification checks like DRC, Density, LVS, Antenna checks.
Tools used:	Cadence Virtuoso Layout Editor, Calibre IC verification tool
Duration	Oct 2017 –August 2019

Project:	**PMR**
Location	ALTRAN Technologies, Bangalore
Client	Intel
Contribution:	*Roles and Responsibilities* ➢ Worked on LDO core block in 16nm Intel Cheetah project. Done area estimation, Floor- plan, matching, Routing, Shielding and done verification checks like DRC, HV DRC and LVS for the same. Also worked on many sub blocks of LDO. ➢ Designed schematics for DUT cells used in PCM based on the layout design for Intel PMR project. Done simulations using cadence spectre tool and calculated the capacitance values for Intel PMR project, parasitic extraction QRC ➢ Worked in TSMC 7nm technology and done power sniffers layout design, extraction, LEF generation for Intel PMR project. In this I did from scratch like placement floor-planning, Routing. Taken care of parasitic in the layout. Did verification checks like DRC, LVS? Metals used were from M0 to M2. Height was H240nm. ➢ Worked in TSMC 6nm technology for Qnr pad rows for Intel PMR project. .
Tools used:	Cadence Spectre , Cadence Virtuoso Layout Editor, Calibre IC verification tool

Project:	**ELASTIX**
Location	HCL technologies ,Hubli
Client	Intel
Contribution:	*Roles and Responsibilities* ➢ Worked in SERDES(Serializer and De Serializer), Floor- plan, matching , Routing, Shielding and done verification checks like DRC, HV DRC, LVS, RV checks in TSMC N5 technology. ➢ Have did the blocks in FB9 layer. have flattened the devices and converted from Fb1 to fb9 layer in standard cell format which is efficient in terms of area, power and performance. Have designed layout for mux and flipflops circuits which were not in the standard cell library. ➢ Maintained symmetry for clock signals routing to match the loads. ➢ Reduced the parasitic like resistance, capacitance, cross coupling for clock signals by shielding. Did strong Power routing for the block. Fixed EMIR for the block. ➢ Did all sub-blocks in SERDES. Tape-out is also successfully done.
Tools used:	Cadence Virtuoso Layout Editor, One LV, Totem

Project:	**TEG**
Location	HCL Technologies,Hubli
Client	Intel
Contribution:	*Roles and Responsibilities* ➢ Have worked on the standard cell blocks of 169nm height in TSMC 3nm. ➢ Have did the floor planning, Routing and verification checks like DRC ,LVS ,TSMC checker(like standard cell layout guidelines, Butting DRC, PIN check), Abutment check, XOR for the cells designed.
Tools used:	Cadence Virtuoso Layout Editor, Calibre IC verification tool

Project:	**Evros**
Location	Wipro Ltd.
Client	Qualcomm
Contribution:	*Roles and Responsibilities* ➢ Have worked on LDO block in TSMC 22nm .Completed the LDO block ➢ Have did the floor planning, Routing and verification checks like DRC ,LVS,DFM checks. Maintained symmetry .Taken care of the power routing. ➢ Did all the subblocks of LDO and top level integration. ➢ Have worked on the cap bank design for VCO. ➢ Have worked for power Amplifier. Taken care to maintain the low resistance. .
Tools used:	Cadence Virtuoso Layout Editor, QVI verification tool

CO-CURRICULAR ACTIVITY

- Presented Hindustani Classical music in All India Radio Dharwad.
- Received Pt. Ranganath Hegde Award for Hindustani Classical Music.
- Presented Music at Karavali Utsav, Sharavati Utsav of Karnataka, and Sawai Gandharva Music festival in kundgol.