Vijay Lakshminarayana

Personal Details:
Birth date: 18 July 1988
Languages: English – Business , Japanese – Conversational, Telugu –Native
Nationality: Indian
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Qualification:
From: 2012 - 2014
University: Amrita Vishwa Vidyapeetam, Bangalore
Degree: Master of Technology (M.Tech)
CGPA: 8.86

From: 2006 - 2010
College: Bangalore Institute of Technology (B.I.T)
Degree: Bachelor of Engineering(B.E)
Percentage: 68.61%

Overview:
Skilled, resourceful and dynamic individual having 7+ years of experience in CMOS Image Sensor domain, Analog/Mixed Signal Circuit and layout designing. Currently looking for a challenging position in Analog domain with an opportunity for growth and career advancement as successful achievements.

Summary of Technical Skills and Experience:

- Familiar with Analog design and analysis technique
  - Can design, verify and simulate CMOS analog blocks for power management circuits including voltage references, bias circuits, comparators, amplifiers and ADC's meeting required specifications.
  - Can perform post layout parasitic extraction and back-annotated simulations to validate design.
  - Can perform requisite Monte-Carlo Analysis on key circuits to ensure 5 Sigma quality and yields.
  - Can initiate experiment to understand Root Cause Analysis and behaviour of the circuit across PVT conditions and propose solutions.
  - Can perform layout for the analog and digital blocks and validate DRC,LVS, COV, DFM and ANT check using Cadence Calibre.

- Analog Circuit Design skills
  - Amplifiers : Single stage- CS, CG,CD
  - Opamp: 2-stage Opamp, Folded Cascode, Telescopic Opamp.
  - BGR:1.2V voltage summing architecture, Fractional type Current Summing Architecture.
  - Bias Generator: V-I converter using internal/external resistor, Cascode Current Mirror Circuits.
  - Ramp Generator: Ramp Generator using Current steering type architecture.
  - ADC architecture: Single Slope RAMP ADC, SAR ADC.
  - LDO Regulator with current sinking/sourcing type.

- Layout Design Skills
  - Can perform layouts for analog blocks considering matching techniques such as common centroid for differential pair and current mirror devices to reduce variation.
  - Usage of metal shielding for critical nets to reduce coupling from other nets.
  - Checking of drawn metal lines strength to avoid Electro-migration.
  - Can draw layouts satisfying design rules for a given process.

- **Tools and Simulators**
  - Cadence Virtuoso
  - ADE/ADEXL/Maestro
  - LVS, DRC : Cadence Calibre
  - Extraction : Start-RC GUI type, Command Type extraction.
  - Simulators: AFS/Spectre/Customsim-XA

Professional Experience

Project 1: Top Level "Column Parallel Single Slope,14 bit ADC for a 35mm Full Frame sensor"
Team Responsibility: Feasibility study of Comparator and S/H blocks with Auto Gain control, RAMP Generator and Counter blocks. Design of bias block for comparator block, modification of RAMP Generator block for given specification, study of Clock repeater circuits for Counter blocks. Preparation of top level schematic for Comparator/SH block, Ramp Generator and Counter block.

My Responsibility:
- RAMP Generator:
  - Complete in-charge of Ramp Generator block. Circuit modification to support different modes and Gain. Modification of Current bias generator block.
  - Perform functional verification of the Ramp Generator block and validate the results.
  - Perform characteristic verification s such as DC-Op check, Amplifier Stability check, PSRR, Noise Analysis, Gain Linearity verification.
  - Layout extraction and back annotation simulations.
  - Layout support, review and feedback to layout team.
- Comparator/SH block:
  - Design of bias block for amplifiers. Perform characteristic verification for bias block.
  - Preparation of top level streaking bench considering layout parasitic and power supply model and perform streaking simulations for different modes.
  - Investigate the reason for large streaking and perform necessary modifications to improve streaking.
  - Layout review and feedback to layout team based on streaking results.
- Counter block:
  - Study of clock repeater circuits to improve clock driving capability.
  - Preparation of DNL budget table to confirm the available clock margin.
  - Preparation of Counter streaking bench and verify the streaking results.
  - Preparation of top level schematic for Counter block

Project 2: Study and modification of "Fractional Band Gap Reference and bias circuit"
My Responsibility:
- Modification of voltage reference circuit to obtain a required band gap voltage.
- Modification of current bias circuit to provide bias current to different bias block.
- Design of Rail-Rail Folded Cascode amplifier. Perform characteristic verification of the Rail-Rail Opamp.
- Perform characteristic verification of BGR block such as voltage/current variation across PVT corners, amplifiers stability check, DC-op check, PSRR, Noise.
- Layout design for the Rail-Rail Opamp

Project 3: Feasibility study of "New architecture of Column parallel SAR-ADC adapted for CMOS Image Sensors"

My Responsibility:

- Performed literature survey to understand the recent advancement in column parallel SAR-ADC adapted for CMOS Image Sensors.
- Design of Pre-Amplifier, Dynamic Comparator and verify AC characteristics of Pre-Amp, Offset measurement, Noise.
- To verify SAR ADC functionality check.
- Various characteristics of SAR ADC was studied such as Gain Variation, Offset, Random Noise, Power Consumption etc., and compared with Single Slope RAMP ADC architecture results.

Project 4: LDO Regulator with current sinking type.

My Responsibility:

- Study of various LDO with current sinking type architectures.
- Verified characteristics of LDO such as dc-op points, load regulation, stability during load/no-load condition, PSRR, Noise.
- Performed layout for regulator block considering matching techniques such as Common Centroid to reduce mismatch.
- Usage of fat metals for large currents and across pass transistor to maintain a low IR drop across pass transistor.
  Layout verification such as DRC, LVS, COV, DFM and ANT check was performed for the drawn layout

Layout Experience

- **Project:** Layout design for "Column Parallel Single Slope,14 bit ADC for a 35mm Full Frame sensor"
  My Responsibility;
  - Performed layout for a comparator column for 2.5um pitch. Considered shielding for critical nets to reduce coupling caps.
  - Performed layouts for bias blocks in Accessory. Used matching techniques for current mirror circuits to reduce mismatch.
  - Modified layout of comparator columns to reduce coupling capacitors based on streaking results.

Career History:

From ; Feb 2015 – Present
Company: Elveego Circuits Pvt Ltd, Bengaluru, India
Designation: Member of Technical Staff
Work: Currently working in client location, Atsugi, Kanagawa as a contract employee in CMOS Image Sensor domain.

From: Nov 2010 – Jul 2012
Company: Tata Consultancy Services (TCS)
Designation: Assistant System Engineer (ASE)
Platform: Dotnet
Project: Was working in conversion project of windows based application from Visual Basic to Visual Basic.NET for Citi Bank client.