Sumit Sharma

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Objective

*Seeking a challenging position in **VLSI Design (To become a best Memory Circuit Design & Characterization Engineer)** apply my creative and design skills towards the organization growth as also to develop myself professionally in this field. Relocation is not a problem*

Executive Summary

- *A dedicated professional with ~8.0 Years of industry experience including Memory Characterization & ASIC Library Development*
- *Working with Tier-1 Semiconductor Clients Microsemi Corporation-Hyderabad, MediaTek Technology-Bangalore, ARM Embedded Technologies-Noida, Qualcomm Inc., Bangalore & EMMicroelectronic-Marin, Switzerland & ZMDI-Germany*
- *Worked on different technology nodes ranging from 28, 45, 65, 90, 130, 180nm, 350nm across various foundries GF, IBM, TSMC, UMC, Samsung, ALP (EMM)*
- *Understanding of SRAM/ROM Memory Architectures*
- *Understanding of Globals/Clock Network Architecture in FPGA-Fabric*
- *Experience in Writing SPICE Deck, Measure Statement*
- *Involved with Characterization for Timing Model using Lib-Char Tools, Generated different view of Library .LIB, LEF, Cir File, RC-Extraction, CDL In, CDL Out, Stream In, Stream Out , Characterization of Cells at different PVT's*
- *Deliverables: .CDL, .GDS, LEF, Front End Models (.vhd, .v), .lib (Liberty File), Validation Report & Documentation*

Technical Expertise

Circuit Design	:	*Schematic Composer (Cadence), Custom Designer (Synopsys), Design Architect (Mentor Graphics)*
Layout Design	:	*Virtuoso (Cadence), IC Station (Mentor Graphics)*
Characterization	:	*HSIM, HSPICE, Finesim (Synopsys), Spectre MDL (Cadence)*
Extraction	:	*Star RCXT (Synopsys), PEX (Mentor Graphics)*
Physical Verification	:	*Calibre (DRC/LVS) Mentor Graphics, Hercules (Synopsys)*
LEF View	:	*Abstract Generator (Cadence)*
Process/Device Simulator	:	*Athena/Atlas Silvaco TCAD*
HDL's Simulators	:	*NC-SIM (Cadence), ModelSim 6.7 (Mentor Graphics)*
HDL's	:	*VHDL & Verilog HDL*
Scripting Languages	:	*Shell, Perl*
Operating Systems	:	*Linux (CentOS, Solaris, Ubuntu), Windows*

Projects Summary

➢ ***Senior Engineer, MosChip Technologies Ltd., Hyderabad*** *(1st June 2018 - Presently)*

Job Profile/Responsibilities:

- *Characterization & Verification of globals (clock network) in Fabric-FPGA*
- *Ran Extractions, Stitched the netlist of globals using Vertu tool*
- *Ran simulations & qualify the timing arcs according to the schematic*
- *Measured clock skew, Qualify the delay by adding cap between the driver & clock input with refrence*
- *Data review of numerous blocks in Fabric (Globals, LSRAM, MATH, PreTime & Routing Buffers)*
- *Documented & Presented the data of Globals in Fabric as per requirements*

➢ ***Senior Engineer, InSilico TechServices Pvt. Ltd., Bangalore*** *(13th Dec., 2017 – 31st May, 2018)*

Job Profile/Responsibilities:

- *IV Curve for NMOS/PMOS across all the corners*
- *Sizing the Inverter & fix the trip point*
- *Measure the delays & rise/fall time*
- *Develop the SPICE Deck for timing measurement in HSPICE*
- *Verification setup & hold time of Latch*
- *Documented & presented*

➢ ***Senior Engineer, Blackpepper Technologies, Bangalore*** *(24th Oct., 2016-12th Dec,, 2017)*

Client: MediaTek, Bangalore

Job Profile/Responsibilities:

- *Ran Extractions (RC)*
- *Compiler views generation (.siz, .gds,.lef, .lib, .verilog,) using Kits_Gen*
- *Timing Characterization using PathChar & Generate TBs*

- *CCSN Characterization & QA @ GF14LPP, T12FFC, TSMC28LP & TSMC28HPM*
- *.lib generation (CCSN) & QA*
- *Full Verification of Compiler @ GF14LPP, T12FFC, TSMC28LP & TSMC28HPM*
- *Wavier Documents for Full Verification*

➢ ***Design Engineer-II, Aricent Technologies, Noida (India)*** *(2nd Dec. 2014 – 24th June,2016)*

Client-ARM Embedded Technologies, Noida
SRAM Memory Compiler at TSMC 28HPM & 28LP
Job Profile/Responsibilities:

- *CDL, GDS & LPE Extraction*
- *Running tilers for various mux options 4, 8, 16, 32 & memory options like redundancy, bmux etc*
- *Clean the setup & Ran simulations for various timing ARC's using ichar tool & tracking & debugging the errors*
- *Static Circuit Check using Calibre PERC*
- *Characterization of memories for timing, power & pin-cap data for different PVT corners*

➢ ***Design Engineer-I, SiCon Design Technologies, Bangalore (India)*** *(May, 2014 – 24th Nov., 2014)*

Client: Qualcomm Inc., Bangalore (India)
Technology: 28nm (LP & HPM), Tools used: Qualcomm Memory Compiler Tools
Job Profile/Responsibilities:

- *CDL, GDS Generation, LPE Extraction (Extraction of RC Netlist)*
- *Simulation firing (Timing & Power) & tracking of the status*
- *Characterization of different parameters such as Access time, Power, Leakage, S/H, Pin-Cap & IV Curve*
- *Pin cap characterization for all the input pins to find how much capacitance is present at the input pin*
- *I-V Characterization for all the output pins of memory*
- *.lib generation using MA & QMRT*
- *Running QA on generated. libs*

➢ ***Design Engineer, RF Silicon Technology, Noida (India)*** *(28th Sept. 2011- 3rd April 2014)*

Characterization of Custom SP SRAM Memory (1Kx16cm8)
Job Profile/Responsibilities:

- *Integration of complete memory*
- *Generation of .CDL, .GDS, .DSPF views of memory*
- *Written measurements for access time, setup & hold time, Pin-Cap, Power (Leakage/Dynamic)*
- *Characterization using HSIM (Timing, Power & Cap)*
- *Leakage Power using Spectre MDL*
- *Functional Verification using NCSIM (Cadence)*
- *Documentation: Technical Datasheet, Validation and QA Report*

➢ ***Characterization of Application Specific Standard Cell Library at 90nm/180nm/350nm***
Job Profile/Responsibilities:

- *Standard Cells Library set cells comprises DFF's, Scan DFF's, Inverter, Buffer, MUX etc. The Layout Design of the same block with via to via grid metal drawing, design in 10 Tracks with power abutment structure.*
- *Primitive Logic Design (AOI, OAI, OR etc)*
- *Sequential Cells Design (Latch and DFF)*
- *Layout Design with 10 Track, 12 Track*
- *Characterized at different process corner*
- *Generating various Views such as .CDL, .GDS, ASCII, .DSPF & LEF*

➢ ***Design and Characterization of 20 Track STSCL Standard Cell Library***
Job Profile/Responsibilities:

- *Layout Design of Inverter, XOR Cells using STSCL logic.*
- *Physical verification of Cells using Calibre & Hercules*
- *RC-Extractions of the cells*
- *Generation of .CDL, .GDS, .DSPF, LEF View of Cells*
- *Characterization of cells using Cadence Spectre MDL*
- *Documentation: Technical Datasheet, Validation and QA Report*

➢ ***Design and Development of Dual Rail Power optimized Standard Cell Library***
Job Profile/Responsibilities:

- *Standard Cells Library set cells comprises DFF's, Scan DFF's, Inverter, Buffer, MUX etc. The Layout Design of the same block with via to via grid metal drawing, design in 10 Tracks with power abutment structure.*
- *Primitive Logic Design (AOI, OAI, OR etc)*
- *Sequential Cells Design (Latch and DFF)*

- *Layout Design with 10 Track, 12 Track*
- *Generating various Views such as .CDL, .GDS, ASCII, .DSPF & LEF*
- *Circuit with Low voltage operation, Characterized at different process corner*

➢ ***Central Electronics Engineering Research Institute (CSIR-CEERI), Pilani (India) Analog Design Intern, IC Design Group*** *(M.Tech. Project) From Jan. to Aug., 2011 Guide: Dr. S. C. Bose (Senior Scientist)*

Title : Analysis & Design of On-Chip DC-DC Converter in AMS 0.35um CMOS technology

Job Profile/ Responsibilities:

- *Deliverables : .CDL, .GDS, LEF, Documents (Project Report, Presentation)*
- *Design of Static, Dickson & Dynamic Charge Pump*
- *Circuit is tested by driving the CMOS Inverter as a Load*
- *Simulation of individuals Architectures using Spectre*
- *Analysis such as Boosting Voltage Analysis, Power-Consumption, Frequency-Variation, Temperature-Variation (-40C to 125C) & Ripple Analysis*

➢ ***Central Electronics Engineering Research Institute (CSIR-CEERI), Pilani (India)***

Research Intern, Sensor & Nanotechnology Group *(M.Sc. Project) From 12 June to 12 Dec., 2008 Guide: Dr. Anil Kumar (Senior Scientist)*

Title : Deposition of Hard Material Nanostructures using Dip-Pen Nanolithography (DPN)

Description: *In this project Silicon Nano-Particles have been deposited on the silicon dioxide (SiO2) substrate using DPN technique at constant temperature and humidity. The deposited silicon nanoparticles layers have been analyzed using NanoRule software & the minimum line width has been observed 30 nm.*

Publications

➢ *A.Kumar, Pankaj B. Agarwal,* ***Sumit Sharma****, D.Kumar, "Nano-Scale Patterning of Silicon Nano-Particles on Silicon Substrate using Dip-Pen Nanolithography", Journal of Nano and Electronic Physics, Volume 3, Number 1, Part 127-131, March 2011.*

Co-Curricular Activities

- *Awarded* ***Second Prize*** *in Paper Presentation on Electronics in* ***National Symposium on Electronics & Technology (NASET-2010)*** *at Kurukshetra University, Kurukshetra (Haryana), India*
- *Participated in two days workshop on* ***"Challenges & Opportunities in Analog & Mixed Signal Design (AMS-2010)",*** *Kurukshetra University, Kurukshetra (HR.)*
- *Organizer & Active Team Member of* ***"QUEST"***
- *Participated in* ***ST-Synopsys*** *University Day Programme, STMicroelectronics, Greater Noida (U.P.), 16thNov.,2010*

Academic Qualification

- ***Master of Technology (Microelectronics & VLSI Design)****, Kurukshetra University, Kurukshetra with 70% in 2011*