Shashank Lingala

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CAREER INTERESTS:

- Analog, Mixed Signal IC Design

PROFESSIONAL EXPERIENCE (8+ years):

Summary

- Experienced Analog Design Engineer with a demonstrated history of working in the semiconductors industry.
- Designs execution and management through consistent tracking of activities and enabling effective communication between the design, verification and layout engineers till GDS.

SKILLS:

Analytical

- Excellent interpersonal communication skills
- Self learner with ability to take initiatives on own

Technical

- Good understanding of analog CMOS design and verification
- Knowledge of layout design techniques, DRC and LVS

Tools

- **EDA tools**: Cadence Virtuoso (Spectre RF, Assura, MDL & Ocean Scripting)
- Hands-on experience with Agilent Spectrum analyzer, signal source analyzer

PROJECTS:

- **CMOS TDI Image Sensor Readout (Luminasic Pvt. Ltd., India: Sep' 2018 ~ present)**

  Responsibilities:
  - Bias Generator verification and design modification to meet the specifications.
  - Pad ring design and Power sequence verification to minimize leakage currents during startup.
  - Array level verification of digital blocks for layout modification to minimize IR drop and bounce.

- **Power on reset (Analog Devices, India: Aug' 2017 ~ Aug' 2018)**

  Responsibilities:
  - Design of a Vt/R reference based POR in TSMC 180nm for use in AMR/TMR automotive sensor.
  - Project management with JAMA, JIRA tools.

- **Low Dropout Regulator (Digicomm Semiconductors Pvt Ltd: Aug' 2017~2018)**

  Responsibilities:
  - Implementation of a low quiescent current LDO regulator with Buffer Impedance Attenuation technique (*ref: IEEE JSSC, Vol. 42, No. 8, August 2007*).
  - Guide junior engineers with implementation and verification (in Tanner EDA tool) and report preparation.

- **CMOS Image Sensor (Elveego Circuits Pvt Ltd: April 2013 ~ July 2017)**
  Responsibilities:
  - R-2R DAC implementation and verification.
  - Verification of various analog blocks.
  - Design library management and interaction with layout engineers.

- **CMOS Image Sensor (SONY, Japan)**
  Responsibilities:
  - Verification of Vertical scanner block
  - HISMCCK check for leak paths, TREC and EM analysis.

- **LVDS Transmitter and Receiver design (TIA/EIA-644 Standard)**
  Responsibilities:
  - Design and verification of LVDS Transmitter and Receiver buffers in Tower Jazz 180nm CMOS technology node for data rates of up to 945Mbps.
  - Design of Built in Self Test (BIST) circuits like fixed pattern generator, PRBS7.
  - Verification of Bandgap Reference and LDO regulator over corners.

- **900MHz Direct Conversion Transceiver Front-end**
  (SM Wireless Solutions Pvt Ltd: January 2012 ~ August 2012)
  Responsibilities:
  - Design of a two stage folded-cascode operational amplifier with rail-to-rail input common mode range in CSMC 0.13um CMOS technology.
  - Implementation of a 5th order Butterworth complex band pass filter (CBPF).
  - Design of a programmable gain amplifier (PGA) with low frequency feedback for DC offset cancellation in CSMC 0.13um CMOS technology.

PUBLICATIONS:

[1] **S. Lingala** et al., "A wide tuning range – 163 FOM CMOS quadrature ring oscillator for Inductor less reconfigurable PLL", IEEE International symposium on Signals, Systems & Electronics 2010, September 17-20, China.***(Nominated for best student paper award)***

[2] **S. Lingala** et al., "A 1.35-6.15GHz linear voltage controlled ring oscillator in 180nm CMOS", IEICE Electronics society conference, C-12-33, September 2010, Japan.

EDUCATION:

- **Master of Engineering (Electrical)** **March 2011**
  (Graduate student at RFIC & Microwave Devices laboratory)
  Kyushu University, JAPAN (GPA --- **3.74 / 4.0**)
- **Bachelor of Engineering in Instrumentation** **June 2008**
  Osmania University, INDIA (Distinction with an aggregate of **76%**)

PERSONAL DETAILS:

Nationality **:** Indian
D.O.B **:** 22nd January 1987
Marital Status: Married
LANGUAGES: English (Professional Level)**,** Japanese (Basic Level)**,** Telugu (Mother Tongue)