RESUME

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Objective:

Skilled, resourceful and dynamic individual, having 5+ years of experience in CMOS Image Sensor domain, Analog/Mixed-Signal Circuit and Layout designing. Currently looking for a challenging position in Analog domain with an opportunity for growth and career advancement as successful achievements.

Education Details:

Class	Year Of Passing	Branch	School/College	Percentage/ CGPA
Master of Technology(M.Tech)	2014	VLSI	Amrita Vishwa Vidyapeetam, Bangalore.	8.86
Bachelor of Engineering(B.E)	2010	Telecommunication	Bangalore Institute of Technology(B.I.T)	68.61

Work Experience:

- **Company :** Elveego Circuits Pvt Ltd, Bengaluru, India
  Designation: Member of Technical Staff
  Duration : 05-Feb-2015 – Present
  Project : Currently working in Sony Corporation, Atsugi, Kanagawa as a Contract employee in CMOS Image Sensor domain.

- **Company:** Tata Consultancy Services (TCS).
  Designation: Assistant System Engineer (ASE)
  Duration: 25-Nov-2010 to 31-Jul-2012
  Platform: Dotnet
  Project: I was working in conversion project of windows based application from Visual Basic to Visual Basic.NET for Citi Bank client.

Technical Skills:

- Have comprehensive knowledge on the concepts, practices and processes of designing. verification and simulation of CMOS analog blocks.
- Experienced in designing of two-stage differential amplifiers, Folded Cascode Opamps, LDO's, Band Gap Reference (BGR) Circuit, Ramp Generators, Counter blocks, SAR ADC.
- Can program efficiently using Hardware Description languages such as Verilog and VHDL.
- Familiar with layout design for Amplifiers blocks considering matching techniques, for digital blocks such as Flip Flops Level Shifters etc,

Design Experience:

- Recently completed the feasibility study of 35mm CMOS Image Sensor project. The studied sensor chip is composed of two stacked chips, Pixel chip and Logic chip. The sensor chip has a pixel pitch of 5.12um and with 4 parallel AD's for each pixel column. AD (CM+SH+CN) has a column pitch of 2.3um for (CM+SH) and 2.1um for CN. The CM+SH and CN column is comprised of 8 ISL's with each ISL having a column of 1800.The control signals to the ISL 's are provided from Accessory block placed in the center of 8 ISL's..

Basic blocks designed//studied during feasibility study are mentioned below

1. **Ramp Generator (DATOP):** DATOP block was modified from the base type of IMX550 and basic features of DATOP block are mentioned below.
   - DATOP block supports various modes such as **Normal mode** (P-phase level: 220mV, D-phase level: 1.22V, Dynamic Range(DR):1V, **Adaptive Gain Control(AGC) mode** and also **Dual Gain mode**.
   - DATOP block supports Analog Gain from 0db-36dB and also has a fine tuning of DR adjustment function..
   - DATOP block has a function to tune POF/Judge with a step of 128LSB each.
   - DATOP supports other features such as Boost function to provide offset during P/D settling, S/H function (aimed at noise reduction), Clock division function, Low Power mode and Test mode to operate DAC in test mode.
   - Other characteristics of DATOP block studied and obtained results was RAMP DNL:0.7 LSB, RAMP INL: 0.08%, Noise: 4.4uVrms @ 0dB(No-AGC), PSRR < -30dB, Setup/Hold Margin of FF's, RAMP Start-up time: 10.5us.

2. **Comparator/Sample & Hold(CM/SH block):** A single slope mode CMTOP block was studied. A S/H block is used to sample and hold VSL signal during P-phase. Some of the other characteristics of CM/SH block are mentioned below:
   - Both CM/SH supports **Auto-Zero** function that perform offset cancellation due to circuit variation. S/H circuit supports feedback type KTC cancellation to reduce random noise of the circuit.
   - CMTOP supports AGC mode thereby providing High Gain(HG) and Low Gain(LG) mode respectively.
   - Other characteristics of CM/SH studied and obtained results was Streaking: 0.9 LSB @0dB, 1.6 LSB @24 dB (Spec: 1 LSB @0dB, 4 LSB @24dB), Streaking Step : 0.04 LSB @0dB, 0.2LSB @24dB, Random Noise : 56.5uVrms @24dB, 103uVrms @0dB, Noise Bandwidth: 2.17MHz @0dB, 705KHz @24dB, Crosstalk : 0.01% in 0dB and 24dB (Spec : 0.12%).

3. **Counter Block(CNTOP):** The CNTOP block was modified from the base type of IMX586. Some of the characteristics of CNTOP block is mentioned below:
   - The CNTOP block consisted of 15 bit GC-Generator. A total of 16 GC-Generators were used for 8 ISL's.
   - A Clock line buffers used in GC-Generators was studied in detail to provide clock to GC-Gen's maintaining characteristics such as Rise/Fall time, Duty Cycle etc.
   - Counter streaking bench was prepared to study the streaking impact due to GC-Gen, Clock Buffers and streaking due to VCO delay and latch in counter columns and obtained streaking was around -0.08LSB.

- DNL Budget was prepared considering DNL of GC-Generators, CLK Line duty, GC delay and margin available was around 95ps considering CLK Frequency of 1.512GHz to Counter block.

- **Bandgap Reference Circuit (BCTOP):** A Fractional BGR circuit was modified from the base type of IMX586. Current summing architecture was used to generate a reference voltage of 0.6V. The modified BGR circuit is currently used in recently released **SONY Alpha1 Full Frame Cameras.**

  Some of the basic features of BGR circuit is mentioned below:

  - BGR circuit has a voltage trimming function with a step of 3mV.
  - Bias currents are generated using V-I circuit. Bias Currents can be generated using Internal Resistor/External Resistor(=47KΩ)
  - The obtained overall variation of BGR voltage across corners is around +/-5% and bias current variation is around -18% to +25% for internal resistor and +/-6% for external resistor.
  - BCTOP block also had Analog/Monitor block to monitor voltages/currents.
  - A **Rail-Rail Opamp** was designed to monitor Voltage Proportional to Absolute Temperature (VPTAT) voltage. A Folded Cascode amplifier was designed to support a Common Mode range from few mV- close to VDD.
  - Other Characteristics of BGR block verified was BGR Voltage Noise: 63uVrms (Spec :76uVrms), Internal Resistor Output Current Noise: 130nArms, External Resistor Output Current Noise: 126nArms (Spec : 4.485uArms), PSRR : -62dB (Spec : <-30dB), BGR Circuit Start-up time : 15ms.

Layout Experience:

1. Rail Rail Op-amp Layout design: For the Rail-Rail Op-amp designed in the BCTOP block, a layout was drawn using ASC11 process. A common centroid matching technique was used for the placement of Input differential pair and current mirror devices. Layout verification such as DRC, LVS, COV check was performed for the drawn layout.

2. Layout design for a LDO block: A LDO block required an reference output voltage of 0.2V and a sinking current of 200mA. To support such large sinking current and to maintain a very low IR drop across a Pass transistor, a layout was drawn considering thick GM metals stacked and used for Pass Transistor routing. Layout verification such as DRC, LVS, COV check was performed for the drawn layout.

3. Drawn layouts for digital blocks such as Level shifters, Flip-Flops and for drivers blocks used in VSCAN block.

Personal Details:

- **Fathers Name:** S.Lakshminnarayana
- **Mothers Name:** M.Vimala
- **DOB:** 18 July 1988
- **Languages known:** English, Japanese (N4 level), Kannada, Hindi and Telugu
- **Residence Address:** 2-1-38, Forest Hills, Room No 205, Oyakita, Ebina, Kanagawa-ken, 243-0419
- **Hobbies:** Listening to music, reading books, watching TV.