NAME: Glen Chen (陳文濱) (Mr.)

SUMMARY:

- ◆ 22+ years experience in analog IC design.
- ◆ 13+ years experience in leading analog design team.
- ◆ 3+ year experience in leading analog layout team.
- ◆ Able to coordinate the design of complex analog functional blocks from creation to production.
- ◆ Experienced in system level design and simulation by MATLAB and C language.
- ◆ Strong grasp in low noise / high linearity / high speed design.
- ◆ Solid signal integrity knowledge and 15+ years on guiding PCB layout for mixed signal / high speed design / low noise design.
- ◆ Willing to do whatever is necessary to get the job done.
- ◆ Industrious in reading books and journal papers.

Date of Birth: 09/10/1969
(*D/M/Y*)

EDUCATION:

Month/Year	**School Name / Degree / Major / Concentration**
06/1995	National Taiwan University / Master / EE / Image Compression
06/1993	National Chiao Tung University / Bachelor / EE

WORKING EXPERIENCE:

1.

Period: 01/2011 – Now
Company Name Weida Hitech / Taiwan.
Position : Director of Analog Design.
Responsibilities:

- ◆ Lead analog design team.
- ◆ Chip ESD protection plan.
- ◆ Touch sensor design guide.
- ◆ Guide System engineer to design PCB for low noise application.

Achievement:

- ◆ Improve first generation AFE SNR and mass production soon.
- ◆ Deliver PLL, USB (full speed) PHY,
- ◆ Deliver dc-dc converters.
- ◆ AIO self capacitance detection AFE, active pen AFE design.

2.

Period: 02/2006 – 01/2011

Company Name Synerchip Technology / Taiwan branch.

Position : Senior Manager / Acting RD Director

Responsibilities:
- ◆ Lead analog design team in Taiwan branch.
- ◆ Lead analog layout team in Taiwan branch.
- ◆ Guide System engineer for high speed PCB design.

Achievement :
- ◆ Work with digital design team to deliver LVDS LCD Timing Controller to LGP company.
- ◆ Lead analog team to deliver Display Port 1.1 RX PHY and license customer in UMC 0.13um process.
- ◆ Lead analog team to deliver HDMI 1.3 active cable booster. (Patent granted in ROC, China and USA)
- ◆ Design IP for Video decoder (10b/175MHz ADC, sync pulse separation) using TSMC 0.18um logic process.
- ◆ Lead USB3.0 PHY IP design using TSMC 90nm LP Logic process (Hands on design on RX Equalizer, TXPLL with SSC).
- ◆ Participate in DiiVA 90nm PHY IP design.

3.

Period: 10/2005 – 02/2006

Company Name Uwave Tech . / Taiwan

Position : Analog Design Manager

Responsibilities:
- ◆ Responsible for the coordination and design of analog integrated circuit for wireless audio application.
- ◆ Responsible to guide PCB layout for low noise..

Achievement :
- ◆ Improvement of existing analog function blocks.
- ◆ Guide PCB layout to achieve high SNDR design.

4.

Period: 07/2001 – 10/2005

Company Name ICPLUS Corp. / Taiwan

Position : Design Manager

Responsibilities:
- ◆ 125MSPS/7bits pipeline ADC maintain.
- ◆ EMI reduction for 5/8 ports Ethernet switch PCB.
- ◆ Design circuit for audio / voice application.
- ◆ Responsible for chip ESD protection plan.
- ◆ Responsible to guide PCB layout.

Achievement :
- ◆ 12 bits sigma-delta ADC design.

- ◆ 10 bit current DAC and speaker driver design.
- ◆ 100MHz/125MHz/166MHz PLL design for VOIP application.
- ◆ 15 bits sigma-delta DAC and headphone driver design.
- ◆ 15 bits sigma-delta ADC design for audio band.
- ◆ Microphone amplifier/bias design.
- ◆ 24.576MHz/3.58MHz XTAL oscillator design.

5.

Period: 01/1998-07/2001

Company name Macronix / Taiwan

Position: Design Engineer

Responsibilities:
- ◆ PLL and data recovery design for 10M/100M Ethernet controller.
- ◆ 100BaseT transmitter design.
- ◆ Production yield improve.

Achievement :
- ◆ Resolve a critical layout bug and improve the production yield for 10M/100M Ethernet controller.
- ◆ PLL and Data Recovery design.
- ◆ 100BaseT Transmitter design.

COMPUTER SKILLS:

C programming , HSPICE , MATLAB , Cadence composer HSIM , Excel , PowerView schematic entry , Design446 schematic entry , Protell .

LANGUAGE ABILITIES: **English:**

Read : Good
Write: Good
Listen: Good
Speak: Good

PROFESSIONAL AFFILIATION:

IEEE member (Solid State Circuit Society)

REFERRER: **Eric Chen - Funder of GrandTek and Weida Hitech (0932-116739)**