Chien-Hung (Brian) Tung

Cellular: 0988007004 Email | brianchtung@gmail.com |
227 Cheng Ging 6th St, Zhubei 302, Taiwan

PROFILE

With solid experience as a process integration, product enabling and yield enhancement owner in developing foundry's process platform and product yield enhancement. Hands on experience on yield and inline, electrical correlation analysis, device yield window definition and chip performance optimization. To coordinate eFA/pFA on advanced Logic, Mixed-Mode, CIS, HV/BCD products to identify the process defect for yield pathfinding. Project management in NPI ramp up, yield improvement, failure and reliability problem solving, DPPM reduction.

EDUCATION

Master of Science, University of Southern California, class of 2003
Major: Electrical Engineering (Electro-Physics), Materials Science
Bachelor of Science, National Chiao Tug University, class of 1997
Major: Electro-physics

ACHIEVEMENT

- Egistec: CMOS Image sensor pixel development, WP and DC improvement (2020)
- Samsung Foundry: 14nm datacenter GPU Yield goal achieved and WLR Pass (2018)
- Intel: 28nm platform development, ramp up BB, RF 5G enabling in foundries (2015)
- Cypress: ULP SRAM and 28/65nm SONOS development. (2012,2013)
- Texas Instruments: 65nm BB, MCU, BCD yield ramp up and DPPM achieved (2008)
- UMC: HiK gate dielectric development and reliability assessment; 65nm SOI process flow set up and device layout design and targeting (2006)

SKILLS

Microsoft OS, Unix, SPC, 8D, FMEA, DOE, JMP, CEDA, Tibco/Spotfire, MATLAB, Labview, Laker, L-edit, K2 viewer, eFA/pFA, Agilent/Keysight 4156 & 4284, ATE.

LANGUAGES

English (Fluent in writing & speaking), Japanese (basic), Mandarin (Native)

EXPERIENCE

Product Technical Manager, Egis Technology, Nov. 2019~May 2020

- To develop 90nm and 65nm FSI/BSI CMOS image sensor process and pixel layout design; process development with the foundry and ML/CF subcontractor for wafer level optics integration and optical performance pathfinding. 0.11um CIS yield monitor and correlation analysis with wafer WAT data.
- 0.18um PMIC product quality assurance, reliability monitor and RMA and failure analysis in subcontractors and wafer foundries.

Principle Product Engineer, Samsung Foundry, Oct 2017-Oct 2019, Austin TX

• Handle customer's 11+/14nm FinFETs GPUs for datacenter and RF products; device corner lots yield analysis, process optimization to achieve the chip performance.

• Bin yield data analysis on customer's 14nm ISP product and inline correlation analysis.

• To lead the yield enhancement and wafer-level reliability qualification and to improve the fails by suggesting the process knob.

Lead Product Engineer/Foundry Manager, Intel Inc., April 2013-May 2017, TW

• 28nm HKMG LP and LPP platform device process integration and devices matching and to solve the silicon and model gap; process and product qualification.

• 16nm FInFETs technology development and x86 CPU ramp up in foundry.

• NPI development and process optimization for yield on 28nm cellular baseband, x86 based mobile CPU (SoFIA), Lighting Peak connectivity and wireless 5G chip and to solve the process and product qualification fails by new process changes.

Sr. Staff Tech Dev. Engineer, Cypress Semiconductor Inc, Dec 2010-April 2013, TW

• 28nm mega SRAM technology development and PCM with yield and SER analysis and to improve the silicon performance with closing the gap with the model target.

• 65nm ULP SRAM and SONOS device corners lots yield window analysis, memory characterization analysis and fails solving and improvement by process change.

Process Integration Engineer, Texas Instruments Inc, Sep 2007-Dec 2010, TW

Device process matching in foundries, PCM and test bin correlation analysis and to drive the foundries for yield enhancement and to reduce burn-in DPPM fails.

• 65nm Cellular BB SoC, MSP, WiLink, ASIC product handling and yield enhancement.

• 0.25/0.35um BCD (LBC7) device process technology transfer and development in foundry with the introduction of foundry design rule and process optimization.

R&D Process Integration Device Engineer, UMC, Sep 2003-Sep 2007, Hsinchu, TW

Advanced technology node of CMOS process technology integration and device characterization to meet the device performance on logic and SRAM devices and to develop the process knobs to achieve the requirement for wafer level reliability.

• High-k dielectrics/metal gate and strain Si process development with module process engineers on gate materials splits for Xtor leakage and performance boost.

• 65nm SOI process flow setup, metrology set up and WAT device analysis.

REFERENCES

1. Ravindra Kapre (VP of Process Tech R&D, Cypress Semiconductor USA),
   Email: rqk@cypress.com , Phone: +1 408 859-0554
2. Chih-Wei Yang (R&D Integration Manager, UMC),
   Email: santoryang@gmail.com , Phone: +886 912-982-352
3. Huy Giang (Product Test Manager, Samsung Austin Semiconductor)
   Email: giang.huy@gmail.com , Phone: +1 832-2355315