**NAME : Takeshi Yanagita**

**Date of Birth : November 2nd, 1972 (Age: 47)**

**Residence : Tokyo Pref. Japan**

**CAREER SUMMARY**

* Over 19 years of experience in electronic component development.
* Over 15 years of professional experience as a CMOS Image Sensor Engineer especially focused on pixel design for more than 13 years (2006 - 2018).
* Experience as a Development Leader for more than 8 years (2 years as a CIS Project Leader & 6 years as a Pixel Design Leader), and responsible for CIS R&D project including the improvement of process integration by cooperating with process integration team.
* 3 years of experience in CIS process structure development.

Core Skills / Experience:

* Experience in the next generation R&D to Product Development of CMOS Image Sensor.
* Skills and experience in Designing CIS Pixel, Layout Design and Simulation.

→Tools: Virtuoso, Spectra, and TCAD

* Knowledge in CIS device and process.
* 5 years of R&D experience in the next generation 180nm CMOS device (SRAM).
* Measurement, Analysis, and evaluation of MOSFET

**PROFESSIONAL EXPERIENCE**

**Sony Corporation, Japan**

**(May, 2003 – July, 2019)**

**January, 2019 – July, 2019**

**Position: Section Chief, Technology Planning**

Main Responsibilities:

* Making R&D technology strategy.
* Studying technology trends.

**April, 2016 – December, 2018**

**Position: Project Leader, CMOS Image Sensor**

Main Responsibilities:

* Performed project milestone, issue and risk management.
* Determined sensor specifications with customer.
* Supervising pixel designers and allocating duties.
* Leader in development of pixels for security applications.

→Formulated mid-term technical roadmap.

**June, 2012 – March, 2016**

**Position: Leader, Pixel Design for high-quality picture development project**

Main Responsibilities:

* Proposed new pixel structures, e.g., DTI structure, pixel of high conversion efficiency and NIR sensor.
* Carried out pixel designing by utilizing process / device simulation, evaluated imaging property of new process and developed items and identified issues.

**April, 2006 – May, 2012**

**Position: Pixel Designer for BSI products**

**(1.65μm 10M, 1.12μm 16M, 1.34μm 16M and1.20μm 20M) for DSC and cellular applications**

Main Responsibilities:

* Designed pixel arrays by using layout tool, produced pixel design rules and performed pixel designing by process / device simulation.
* Handled pixel characteristic evaluation, analysis of defects, cause analysis by utilizing simulation.
* Created and evaluated TEG for pixel transistors.
* Improved pixel characteristics with process integration team.

**May, 2003 – March, 2006**

**Position: Engineer for backside illumination device development**

**M**ain Responsibilities:

* Conducted new process structure development, e.g., inter-pixel light blocking structure, light condensing structure and PAD insulated structure.
* Carried out reliability analysis of new process and took necessary measures.

**Epson Corporation, Japan**

**(April, 1998 – April, 2003)**

**Position: Engineer for Development of SOI transistor technology for SRAM cells**

Main Responsibilities:

* Created and evaluated of TEG for transistors, designed transistors by using simulation (Tsuprem4, medici), performed SPICE model extraction, process flow setup with process integration team, evaluation of transistor characteristics and reliability evaluation of transistors and gate films.

**ACADEMIC QUALIFICATIONS**

**Graduate School of OSAKA UNIVERSITY March, 1998**

**Master of Science in Chemistry**

**OTHER INFORMATION**

**Languages :**

**JAPANESE :** Native Language

**ENGLISH :** Conversational - Business Level

\*Business level in reading / writing, conversational in verbal.