Muhammad Shamookh

Analog Design Engineer

PERSONAL INFORMATION

DOB: 1 March 1999

Bergwinkel, 3,
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SKILLS

- Cadence Virtuoso
- Verilog-A (Basic)
- MATLAB
- Latex
- Proteus PCB Development
- MS Office (MOS Certified)

LANGUAGES

- English (C1)

ABOUT ME

Skillful, articulate professional and team player. Skilled in analog design from project works and student tutor position. Experience in Cadence Virtuoso simulation tool. Worked with Verilog-A in Cadence. Looking to enhance my skills in analog design in a dynamic environment.

EDUCATION AND TRAINING

OCT 2021 – CURRENT

M.Sc. Microelectronics and Microsystem

Hamburg University of Technology (TUHH)

AUG 2016 – SEP 2020

BSc. Electrical Engineering

Government College University Faisalabad, Pakistam

Final grade 1.3

WORK EXPERIENCE

16 SEP 2022 – CURRENT

Analog Design Engineer

Hamburg University of Technology (TUHH)

- Design pixel circuits 2T1C, 4T2C current and voltage programmed in cadence and analyzing the results in 180nm process.
- Design and verify diode model and characteristics with verilog-A in cadence.
- Design input power stage for driving application in brain implants with 180nm XFAB isolated technology
- Researching for designing display intialiy with 4x4 matrix along with input stage.

15 APR 2023 – CURRENT

AICD Tutor

Hamburg University of Technology (TUHH)

- Presenting tasks and assisting students lab meetings on Cadence Virtuoso.
- Conducting exercises for groups of 20-30 students.

PROJECTS

- Cadence design for 90dB 2-stage OpAmp with a compensation network for UGF > 1MHz.
- Layout design for 2-stage OpAmp with LVS verification and parasitic extraction using Cadence.
- 1uA Beta-Multiplier design with startup circuitry under 50uW power consumption with an OpAmp