CONTACT DETAILS

Tokyo , Edogawa-Ku ,
Funabori 6-5-3-101

lakshmi.asokan@outlook.com

+81-7077803682

NATIONALITY

Indian

SKILLS

Tools : Cadence Virtuoso ADEXL/XL, Cadence Spectre Synopsis HSPICE

Scripting: PERL

HDL: Verilog

Circuits: Operational Amplifiers, BGR, Comparator,CTLE

LANGUAGES

English (full working proficiency)

Japanese (Beginner)

LAKSHMI ASOKAN

ANALOG DESIGN ENGINEER

PROFILE SUMMARY

- 2.7 years of Experience in Analog Circuit Design.
- Predominantly worked on Design and Verification of Operational Amplifiers, Bandgap Reference, CTLE etc.
- Knowledge of Analog/ Mixed Signal/ Digital CMOS circuits, CMOS fabrication process and CMOS device physics
- Proficient in using Cadence "Virtuoso" ADE-L and ADE-XL for schematic design.
- Well aware of QRE flows like aging, burning, EOS checks.
- Well aware of the IEEE guidelines for Quality IP Design and Verification.
- Able to manage the delivery of project work on time and also involved in Tape-out's
- Basic Automation using PERL.
- Basic knowledge of CMOS image Sensor.

EDUCATIONAL HISTORY

Master of Engineering VLSI Design
Anna University, Chennai, Tamil Nadu, India

Bachelor of Technology Electronics and Communication Engineering
MG University, Kottayam, Kerala, India

EMPLOYMENT HISTORY

Analog Design Engineer, Cerium Systems, Bangalore,India
DEC 2017- JUNE 2020

Data Receiver and Receiver Bias Generation Circuit for DDR4/LPDDR4
Technology Node: 10nm Fin-FET

- Design and verification of constant gm bias circuit which is used as Receiver bias in DDR4/LPDDR4.
- Performed simulation for characterization (test for min eye width/eye height, test for min eye width/eye height with CTLE enabled, Vref wakeup time, RX Bias wakeup time, RX Bias generation) across PVT.
- Performed analog reliability analysis Aging and Burn-in also Monte Carlo Simulation to estimate statistical performance of a circuit.

Verification of LPRX data path in MIPI-DPHY IP
Technology node: 14nm Fin-FET

- Implemented offset cancellation technique at data receiver and verified the data receiver
- Created test cases for data path
- Performed Monte Carlo Simulation to obtain statistical performance of the circuit after implementation of offset circuit.

Low Dispersion comparator
Technology node: 130nm CMOS

- Design of high speed low dispersion comparator used as a sub block of optical receiver channel.
- Design reduces the propagation delay dispersion caused by variable input overdrive and the common mode level.
- The effect of process variations on the performance of the proposed technique is studied by Monte Carlo simulations